(a) What is the *memory data register*?

1. Describe the main constituents of a typical *control unit*.
2. Compare and contrast *microprogrammed* and *hardwired control units*.
3. Suppose that the instruction set of a machine has three instructions: *Inst-1, Inst-2* and *Inst-3*; and A, B, C, D, E, F, G and H are the control lines. The following table shows the control lines that should be activated for the three instructions at the three steps T0, T1 and T2.

|  |  |  |  |
| --- | --- | --- | --- |
| Step | Inst-1 | Inst-2 | Inst-3 |
| T0 | A, B, G | F, H, G | F, C |
| T1 | G, A | A | B, C |
| T2 | B, C | H, D |  |

Using Hardwired approach:

(i) Write Boolean expressions for all the control lines B, C, D, G. (ii) Draw the logic circuit for each control line.

(e) What is semantic gap as elucidated in *RISC/CISC* evolution cycle?

(f) Highlight the common characteristics of *RISC*-based machines.

(g) Explain the two design alternatives experienced in early design architecture of computer systems.

(h) What constitutes a carefully selected reduced set of instructions in *RISC* based machines?

(i) What is the distinguishing factor among *input devices*.

(g) Describe, in detail, the concept of *shared I/O arrangement*.

(k) Highlight the distinguishing characteristics between *Daisy Chain Bus Arbitration* and *Independent Source Bus Arbitration*.

(l) Discuss the concept of *context switching*.

(m) With the aid of a suitable diagram, explain the operational process of a *2-bus* organization. (n) With the aid of an illustration, state the procedure involved in realizing a typical and simple execution cycle of an instruction in the *CPU*.

(o) In a simple *CPU*, an instruction adds the contents of memory location *X* to register *R0* and stores the result in *R0*.

(p) Highlight the sequence of steps involved in executing the *arithmetic* operation;

(q) How can the arithmetic operation be realized in *two-bus* organization by using micro- operation?

(r) What is *Von Neumann Architecture*?

(s) Discuss the characteristics of *shared memory architecture*?

(t) Explain *Flynn's Classical Taxonomy* in the conceptualization of different classifications of computer systems.

(u) Differentiate between *Single Instruction Stream, Single Data Stream* and *Multiple Instruction Stream, Multiple Data Stream*.